REMARKS

This paper is responsive to the Final Office Action dated October 26, 2005. Claims 1-28 were examined, all of which were rejected. Applicants have concurrently filed herewith a Request for Continued Examination. Applicants have amended independent claims 1, 10, 19 and 23 and have added new claims 29-32 to claim disclosed subject matter that was not previously explicitly claimed. The subject matter of claims 29-32 is fully supported by Applicants' specification, as filed. Applicants respectfully request that the Examiner approve entry of this amendment. Claims 1-32 are now present in this application.

In the present Office Action: claims 1-2, 4-11, 13-24 and 26-28 were rejected under 35 U.S.C. §102(a) as anticipated by U.S. Patent No. 6,829,713 (hereinafter "Cooper"); and claims 3, 12 and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Cooper.

Applicants submit that independent claims 1, 10, 19 and 23, as amended, are not anticipated or obvious in view of Cooper. More specifically, with respect to claims 1, 19 and 23, while Cooper discloses a technique that may skip a performance state, depending upon CPU utilization, Cooper does not teach or suggest always skipping at least one intermediate performance state that is between a current performance state and a predetermined performance state. Furthermore, with respect to independent claim 10, as amended, Cooper does not teach or suggest skipping an intermediate performance state that has a greater associated integrated circuit utilization than a current performance state.

According to Cooper (see Fig. 6), assuming that CPU utilization was previously less than or equal to twenty percent and the CPU utilization increases to greater than or equal to ninety-five percent, the CPU switches from a battery optimized mode (w/o signal throttling) to a maximum performance mode. However, Cooper does not skip at least one intermediate performance state, when switching from the battery optimized mode (w/o signal throttling) to a maximum performance mode. That is, the Cooper battery optimized mode (w/ signal throttling), while being a "maximum battery mode," is a lower CPU performance state than the battery optimized mode (w/o signal throttling). Assuming arguendo that systems that comprise more than three performance states are well known, even if Cooper included more than three performance states, Applicants respectfully submit that Cooper still does not teach or suggest

always skipping at least one intermediate performance state. Nor does Cooper teach or suggest skipping an intermediate performance state that has a greater associated integrated circuit utilization than a current performance state. For at least the reasons set forth above, Applicants respectfully submit that independent claims 1, 10, 19 and 23 are allowable over Cooper.

With respect to new dependent claims 29-32, Cooper teaches throttling (as noted above), which teaches away from the subject matter of claims 29-32 (see Applicants' Background for a discussion as to the disadvantages of throttling). Additionally, Applicants submit that claims 2-9, 11-18, 20-22 and 24-32 are also allowable for at least the reason that they depend upon allowable claims.

Claims 1-32 are in the case. All claims are believed to be allowable over the applied art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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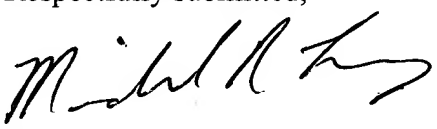

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